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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/763,087

01/22/2004

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17403US05

6408

23446 7590 02/02/2010
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EXAMINER

HASSAN, AURANGZEB

ART UNIT

PAPER NUMBER

2182

MAIL DATE

DELIVERY MODE

02/02/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/763,087	Applicant(s) MACINNIS ET AL.	
	Examiner AURANGZEB HASSAN	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 January 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4,5,7-10 and 12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 4,5,7-10 and 12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/4/2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 4, 5, 7 – 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Yoseph. et al. (US Patent Number 5,949,439, hereinafter “Ben”) in view of Robinett et al. (US Patent Number 6,351,474, hereinafter “Robinett”) further in view of Ottinger (US Patent Number 6,070,231).**

4. As per claim 4, Ben teaches a unified memory system comprising: a memory (buffer memory, figure 2) that is shared by a plurality of devices including at least a

Art Unit: 2182

central processing unit (host processor 102, figure 1) and a graphics processing unit (multimedia processor 106, figure 1); and a memory request arbiter coupled to the memory (resource manager 308, figure 3), wherein the memory request arbiter performs real time scheduling of memory requests from different devices having different priorities (column 7, lines 10 – 21), the unified memory system provides for real time scheduling of tasks (308 dictates control of 310 allowing for real time scheduling column 7, lines 17 – 20), and provides access to memory by requesters that are sensitive to latency and do not have determinable periodic behavior (column 8, lines 22 – 36).

Ben does not explicitly disclose a predetermined delay between subsequent accesses.

Robinett teaches a unified memory system wherein a predetermined minimum interval between subsequent accesses by a device is enforced, and wherein said predetermined minimum interval is long enough for another device to access (predetermined delay is enforced to allow for sufficient adjustment between subsequent scheduled accesses, column 7, lines 50 – 67).

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify Ben with the above teachings of Robinett. One of ordinary skill would be motivated to make such modification in order to adjust scheduling of a multi-request handling system, column 7, line 63 to column 8, line 7).

Ben teaches a unified memory system comprising dual memory controllers, the dual memory controllers including a first memory controller (154, figure 1) and a second

memory controller (156, figure 1) coupled to a memory arbiter performing real time scheduling (308, figure 3).

Ben/Robinett does not explicitly disclose a first and second memory controller coupled to a first and second arbiter.

Ottinger teaches a memory system comprising dual memory controllers (figure 1), the dual memory controllers including a first memory controller (24a, figure 1) and a second memory controller (24b, figure 1), the memory request arbiter including a first arbiter (59A, figure 2) coupled to the first memory controller and a second arbiter (59B, figure 2) coupled to the second memory controller, wherein the first arbiter and the second arbiter perform real time scheduling of memory requests (column 18, lines 34 – 38), wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter based on the address of the memory request (arbiter utilizes address of memory request, figure 2)

It would have been obvious to one of ordinary skill in the art at the time of the Applicant's invention to utilize the dual memory controller/interface of Ottinger in the above mentioned teachings of Ben/Robinett. One of ordinary skill would be motivated to make such modification in order to increase the performance of the system by reducing the average latency of memory requests (column 2, lines 10 – 25).

5. Ben modified by the teachings of Robinett/Ottinger as seen in claim 4 above, as per claim 5, Ben teaches a unified memory system wherein the central processing unit and the graphics processing unit are sensitive to latency and do not have determinable

Art Unit: 2182

periodic behavior (processing does not have periodic behavior, and aims to reduce latency in processing thereby disclosing latency, column 4, lines 47 – 49).

6. Ben modified by the teachings of Robinett/Ottinger as seen in claim 4 above, as per claim 7, Robinett teaches a unified memory system further comprising a circuit component associated with one or more devices and coupled between the associated devices and the memory request arbiter, wherein the circuit component is used to enforce at least a predetermined minimum interval between subsequent accesses by the associated device to the memory (processor circuit introduces predetermined delay between subsequent accesses, column 7, line 50 to column 8, line 7, Ben: teaches access to the memory).

7. Ben modified by the teachings of Robinett/Ottinger as seen in claim 4 above, as per claim 8, Robinett teaches a unified memory system wherein the devices associated with the circuit component include a CPU (Robinette: processor 21, figure 1; Ben: process controller 202, figure 2).

8. Ben modified by the teachings of Robinett/Ottinger as seen in claim 4 above, as per claim 9, Robinett teaches a unified memory system wherein the devices associated with the circuit component make high priority service requests to access the memory through the circuit component (column 40, line 58 – column 41, line 34, circuit processor utilized to make high priority service requests. Ben: teaches access to the memory).

9. Ben modified by the teachings of Robinett/Ottinger as seen in claim 4 above, as per claims 10 and 12, Robinett teaches a unified memory system further comprising a round robin server for handling low priority tasks (column 28, lines 20 – 23, as per claim 12, handles only low priority based upon data utilized).

Response to Arguments

10. Applicant's arguments with respect to claims 4, 5, 7 – 10 and 12 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues newly amended limitations for which the Examiner has provided a new citation from Ottinger for specific teachings required by the arbiter.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AURANGZEB HASSAN whose telephone number is (571)272-8625. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on 571-272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2182

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

/Tariq Hafiz/

Supervisory Patent Examiner, Art Unit 2182